IN THE CLAIMS

Please cancel Claims 1-6 and 8-27, and enter Amendments to, and Allow Claim 7.

CLAIMS 1 - 6 (canceled).

7. (currently amended): An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems, said inverting gate voltage channel induced semiconductor device being formed in a compensated semiconductor epi-layer or substrate characterized by a selection from the group consisting of:

> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and
>
> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

said inverting gate voltage channel induced semiconductor device comprising two junctions, termed source and drain, which are separated by a first semiconductor channel region, and further comprising two additional junctions, termed source and drain, which are separated by a second semiconductor channel region, wherein gates, to which semiconductor channel region effecting voltage can be applied, are associated with each of the first and second semiconductor channel regions, said gates

being offset from said first and second semiconductor channel regions by insulating material;

such that during use application of a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will attract holes to said first and second semiconductor channel regions, the purpose of applying such gate voltage being to affect field induced effective doping of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying when sufficient field induced effective doping is present in the channel region adjacent thereto, and which drain junctions are each rectifying when sufficient field induced effective doping is present in the channel region adjacent thereto;

in which inverting gate voltage channel induced semiconductor device the drain junction associated with said first semiconductor channel region is electrically interconnected with the drain junction associated with said second semiconductor channel region, and in which said gates associated with said first and second channel regions are electrically interconnected;

such that during operation the electrically noninterconnncted source junctions are held at different voltages, and application of a gate voltage affects semiconductor channel region effective doping in said first and second channel regions by field induced means, and thus which electrically interconnected rectifying drain junction in said semiconductor forms, as a result of semiconductor type field induced by said applied gate voltage, and forward conducts, thereby controlling the voltage present at the electrically interconnected drain

junctions essentially through said formed forward conducting rectifying drain junction;

the basis of operation being that the drain junctions associated with said first and second semiconductor channel regions are comprised of at least one material that forms a rectifying junction to a semiconductor channel region when ~~it~~ said semiconductor channel region is caused to be either N or P-type by field induced means, and the presence of at least partially compensated semiconductor which comprises both N and P-type carriers enables easy provision of N and P-type channel region forming carriers via gate voltage application effected field effect means[[.]];

said semiconductor channel region and, when formed, adjacent drain junction which is not forward conducting, being characterized by at least one selection from the group consisting of:

a. being functionally comprised of two regions across which voltage can drop, namely an onset of pinch-off region and a channel region;

b. being functionally comprised of three regions across which voltage can drop, namely an onset of pinch-off region, a portion of the channel region which is populated with some gate voltage field induced carriers, and a formed reverse biased rectifying junction.

CLAIMS 8 - 27 (canceled):

28. (new claim): An SCR-like device formed in a compensated semiconductor epi-layer or substrate characterized by a selection from the group consisting of:

> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and
>
> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

said SCR-like device comprising a semiconductor channel region and a region of material which forms a rectifying junction with both N and P-type semiconductor whether metallurgical or field induced, wherein a gate, to which semiconductor channel region effecting voltage can be applied, is associated with said semiconductor channel region, said gate being offset from said semiconductor channel region by insulating material;

such that in use a DC voltage is applied across said semiconductor channel region and said region of material which forms a rectifying junction with both N and P-type semiconductor whether metallurgical or field induced; and

no voltage, or a voltage which is of a polarity appropriate to attract carriers into said channel region such that a reverse biased junction is formed between said semiconductor channel region and said region of material which forms a rectifying junction with both N and P-type semiconductor whether metallurgical or field induced, is applied to said gate to the

end that substantially no current flows through said semiconductor channel region and said region of material which forms a rectifying junction with both N and P-type semiconductor whether metallurgical or field induced; and

such that when a voltage which is of a polarity appropriate to attract carriers into said channel region such that a forward biased junction is formed between said semiconductor channel region and said region of material which forms a rectifying junction with both N and P-type semiconductor whether metallurgical or field induced is applied to said gate significant current flows through said semiconductor channel region and said region of material which forms a rectifying junction with both N and P-type semiconductor whether metallurgical or field induced.

29. An SCR-like device as in Claim 27 which comprises half of an inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems, said inverting gate voltage channel induced semiconductor device being formed in a compensated semiconductor epi-layer or substrate characterized by a selection from the group consisting of:

said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and

said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping

levels;

said inverting gate voltage channel induced semiconductor device comprising two junctions, termed source and drain, which are separated by a first semiconductor channel region, and further comprising two additional junctions, termed source and drain, which are separated by a second semiconductor channel region, wherein gates, to which semiconductor channel region effecting voltage can be applied, are associated with each of the first and second semiconductor channel regions, said gates being offset from said first and second semiconductor channel regions by insulating material;

such that during use application of a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will attract holes to said first and second semiconductor channel regions, the purpose of applying such gate voltage being to affect field induced effective doping of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying when sufficient field induced effective doping is present in the channel region adjacent thereto, and which drain junctions are each rectifying when sufficient field induced effective doping is present in the channel region adjacent thereto;

in which inverting gate voltage channel induced semiconductor device the drain junction associated with said first semiconductor channel region is electrically interconnected with the drain junction associated with said second semiconductor channel region, and in which said gates associated with said first and second channel regions are electrically interconnected;

said half of an inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems being one selection from the group consisting of:

said first semiconductor channel region; and
said second semiconductor channel region;

and the drain junction associated with said selected first or second semiconductor channel region.

30. (new claim): An SCR-like device as in Claim 28, in which said insulating material which offsets said semiconductor channel region from said gate comprises fero-electric material.

31. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems, in which said insulating material which offsets said first and second gates from said first and second semiconductor channel regions respectively, comprises fero-electric material.

It is now believed that the Application is in order for Allowance, therefore the Examiner is respectfully requested to provide the Notice of Allowance.

Sincerely,

JAMES D. WELCH

JW/hs